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REPORT NO. 119

SOME MEMORY ELEMENTS USED IN ILLIAC II

by

P. V. S. Rao

June 21, 1962

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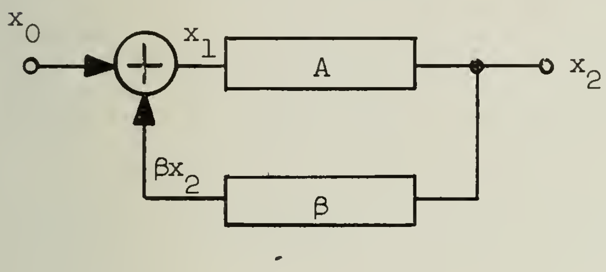
INTRODUCTION

Justification for the existence of this document arises from the fact that while the memory elements in use in ILLIAC II are significantly dissimilar to the standard types in existence elsewhere, they bear sufficient similarity between themselves to make collective discussion possible and reasonably connected. Hopefully, information presented in the following pages will eliminate or minimize the difficulty experienced by an individual not necessarily familiar with this machine, in understanding the functioning of various circuits using these elements. Also, it is hoped that choice of memory elements for new circuits, and circuit design of these memory elements (using, say, new transistor types and/or supply voltage levels) will be simplified to the extent that the relevant information is available from a single source, to afford easier comparison.

Completeness of the information is limited to presentation of a description of a basic model of each type of memory element, its use, and a brief description of its variations, if any. Limitations on design, application, etc., are also enumerated whenever considered desirable. A reasonably complete list of source material is appended at the end to facilitate efforts to find more information in one or more specific categories.

General Discussion

The existence of two stable states under the same environmental conditions implies that flipflops or memory elements exhibit hysteresis. The degree of stability and consequently the ease with which a flipflop can be made to change from one state to the other depend on the magnitude of this hysteresis. A flipflop is conventionally regarded as a regenerative amplifier of the type shown in Figure 1.



The effective overall gain of the amplifier between the terminals x_2 and x_o can be seen in this case to be

$$\frac{x_2}{x_o} = A* = \frac{A}{1-\beta A} .$$

Figure 1

Assuming that the output is limited to $\overline{x_2}$ and $\underline{x_2}$ by non-linearity in the system, the characteristics for the three cases when $\beta A < 1$, $\beta A = 1$, and $\beta A > 1$ are as follows:

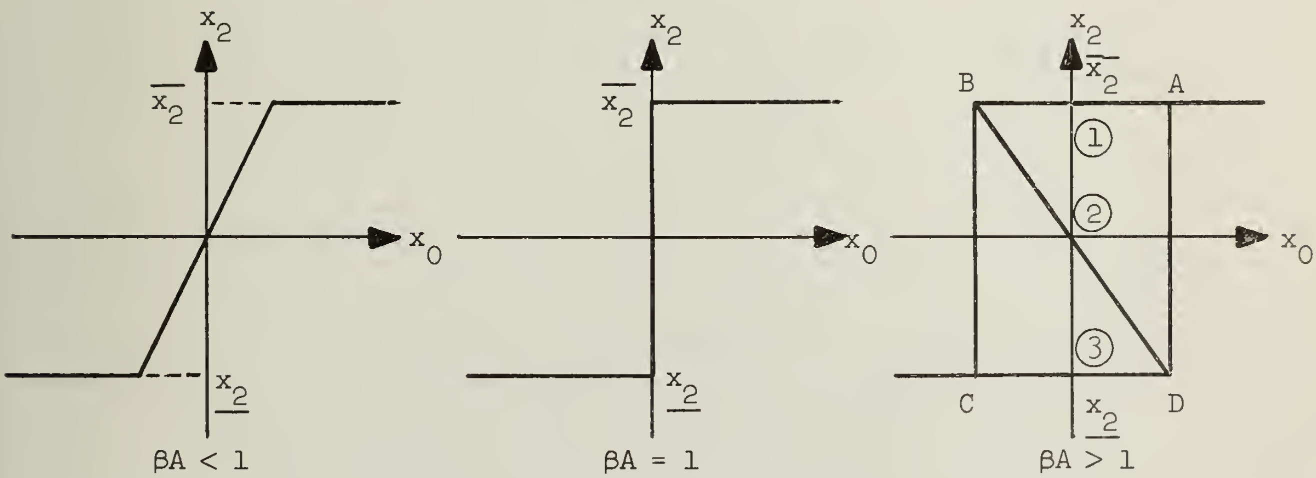


Figure 2

The setup can be seen to have three states of equilibrium ①, ②, and ③ only in case $\beta A > 1$. When $\beta A < 1$, the system is effectively a stable amplifier. When $\beta A = 1$, the system exhibits infinite gain, and an arbitrarily

small signal can drive the output from $\overline{x_2}$ to $\underline{x_2}$. When $\beta A > 1$, there are three equilibrium states marked ① , ② , and ③ in Figure 2. That state 2 is unstable is evident from the fact that any small deviation of the value of x_1 from 0 will result in an accelerated movement to either $\frac{\overline{x_2}}{A}$ or $\frac{\underline{x_2}}{A}$, so that x_2 settles at either $\overline{x_2}$ or $\underline{x_2}$. x_1 finally settles at $\beta\overline{x_2}$ or $\beta\underline{x_2}$

A pulse of magnitude $\frac{\underline{x_2}}{A*}$ makes the flipflop go from state 1 to state 3, and a pulse of magnitude $\frac{\overline{x_2}}{A*}$ takes it from 3 back to 1. If x_o is moved back and forth between $\frac{\overline{x_2}}{A*}$ and $\frac{\underline{x_2}}{A*}$, the circuit moves in the cycle ABCDA.

The width of the hysteresis loop depends on the slope of the amplifier characteristic, and is a measure of the stability of the flipflop.

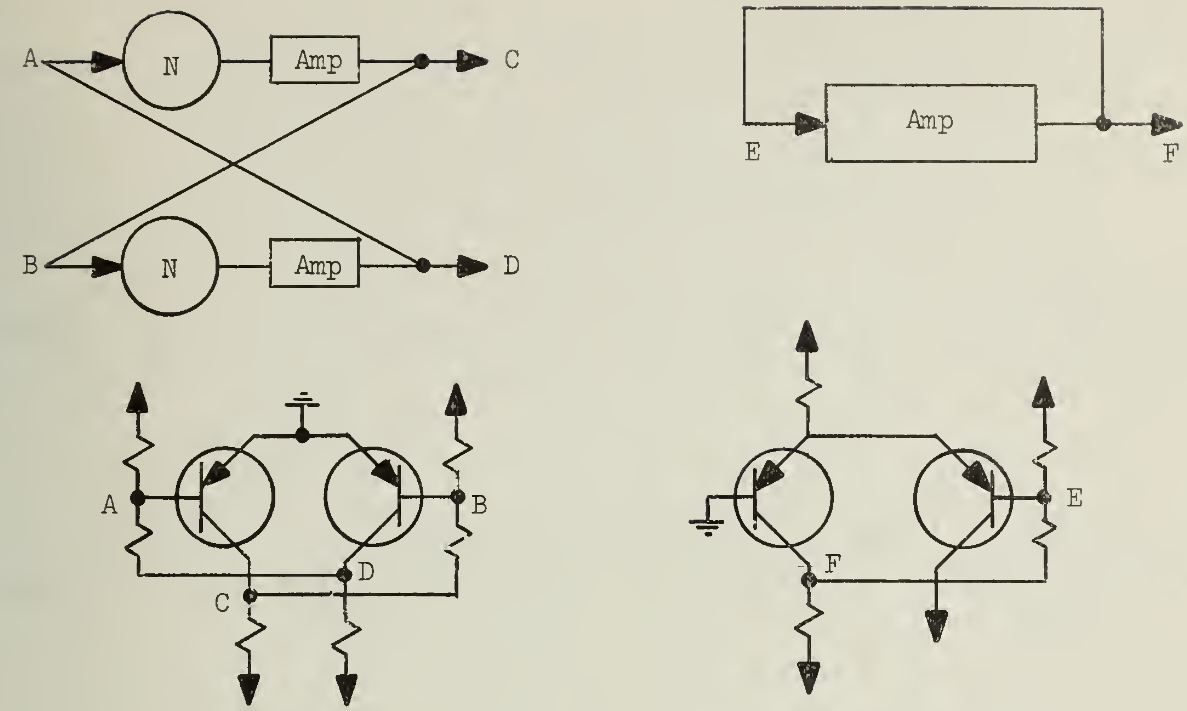
The main conclusions to be drawn from the above discussion are that for flipflop action:

1. Positive feedback is necessary and
2. The loop gain ($A\beta$) must be greater than 1.

Basic Flipflop

The conclusions arrived at in the last section enable one to construct flipflops out of logical elements. Figure 3 gives two basic types of flipflops.

It can easily be verified that either of the two circuits satisfies the conditions imposed by the previous section. The fact that neither of these circuits has an input terminal analogous to x_o in the previous section doesn't impair their action as two state devices in any way. The two stable states of each circuit are enumerated in the diagram. In the absence of convenient input points, the circuits can be made to change state by changing the state of any of the nodes by brute force methods. It can be seen that these diagrams represent the more commonly used flipflops of the standard type (Eccles Jordan or symmetrical flipflops, and the asymmetric or Schmidt type).



Node	A	B	C	D
State 1 ($V_A > 0 > V_B$)	1	0	0	1
State 0 ($V_A < 0 < V_B$)	0	1	1	0

Node	E	F
State 1 ($V_E > 0$)	1	1
State 0 ($V_E < 0$)	0	0

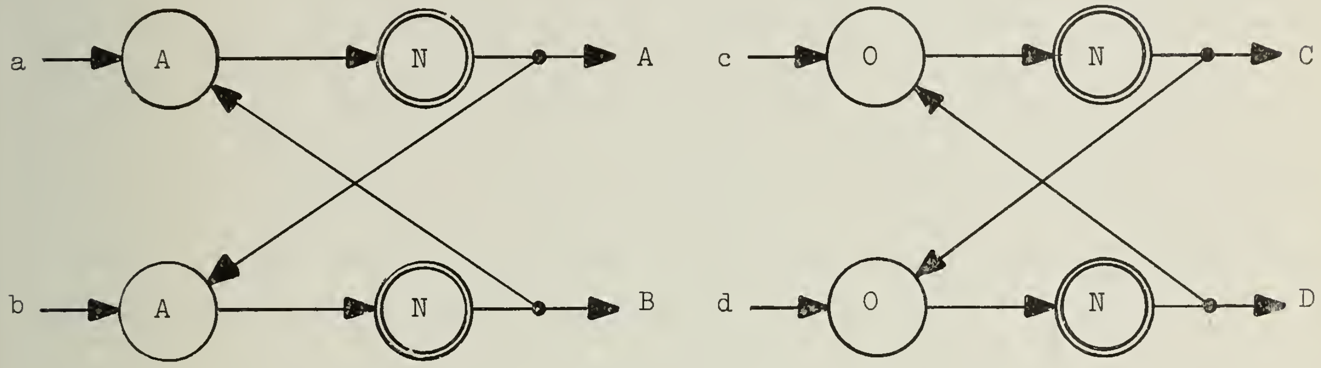
Figure 3

Change of State

Rather than consider the flipflop as changing its state by the use of brute force, it is simpler to visualize the following method: If the feedback loop of a flipflop is broken at some convenient point, it will either take on some intermediate state or run to one or the other of its two stable states. If the desired signal is now impressed at this point, and the feedback loop rejoined after a suitable delay the flipflop will hold this new state. This process consists of replacing the feedback signal by the input signal during the gating time. The flipflops of Figure 3 have been modified to incorporate this feature in Figure 4.

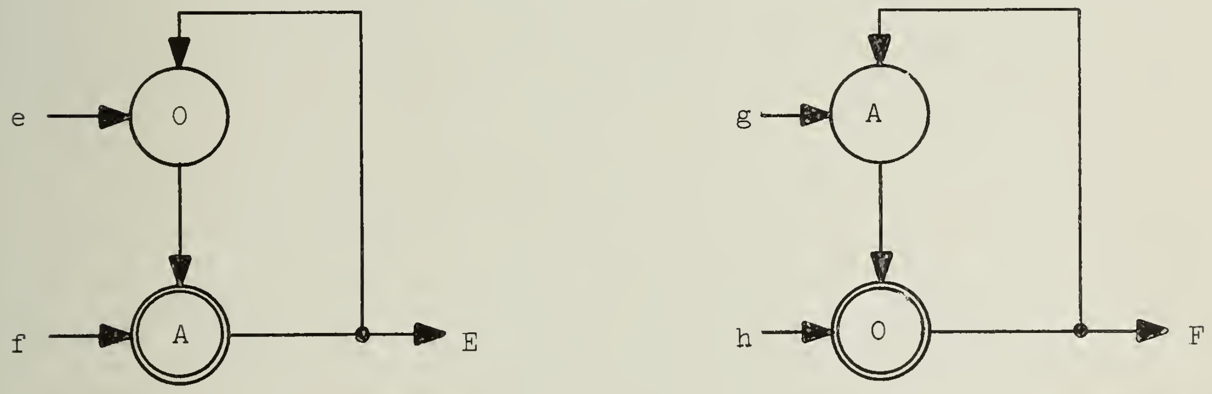
Firstly, new logical elements have been introduced in the feedback loop to enable it to be broken when desired. Secondly, the separate amplifiers are eliminated by using restoring circuits which besides performing their intended logical operation, amplify the output and bring it back to standard levels.

The inputs that have now been provided can be seen to perform the function of both disconnecting the feedback chain and impressing the desired signal value into the flipflop at the same time. An input to any of these flipflops is defined to be in the quiescent state when it does not cause the feedback loop to be disrupted, and in the active state otherwise.



4.a.1 And Not Eccles Jordan

4.a.2 Or Not Eccles Jordan



4.b. Schmidt Type

4.c. Schmidt Type

Figure 4

The ultimate behavior of a flipflop when both inputs become simultaneously active is not immediately obvious. This would, as even in the case of a single active input, disrupt the feedback loop. The final state of the flipflop is that in which it remains just prior to the time the feedback loop is rejoined. Thus, for unambiguous behavior, one of the inputs has to persist longer than the other for a time equal to or greater than the response time of the flipflop. In this case, an equilibrium state is attained before the remaining signal also returns to its quiescent state. The input signal, in the process of returning to its quiescent state, rejoins the

feedback loop and locks in the new state. If this condition is not satisfied (an extreme case being one in which both the inputs return to the quiescent state simultaneously), a race condition exists and the final state of the flipflop is undetermined.

In Figure 4.b. for example, a 1 at e and a 0 at f would result in a 0 at E but a 1 at the output of the "OR". Clearly, the feedback loop has been disrupted. The final stable state attained by the flipflop depends on the response time of the flipflop and the delay between the times the two inputs return to their quiescent states. If in the above example, e returns to 0 first, and f returns to 1 after a certain delay, the final state of the flipflop is 0, provided this delay is equal to or greater than the response time of the flipflop. If it is less, a race condition exists. Similar statements can be made in connection with the other flipflops as well.

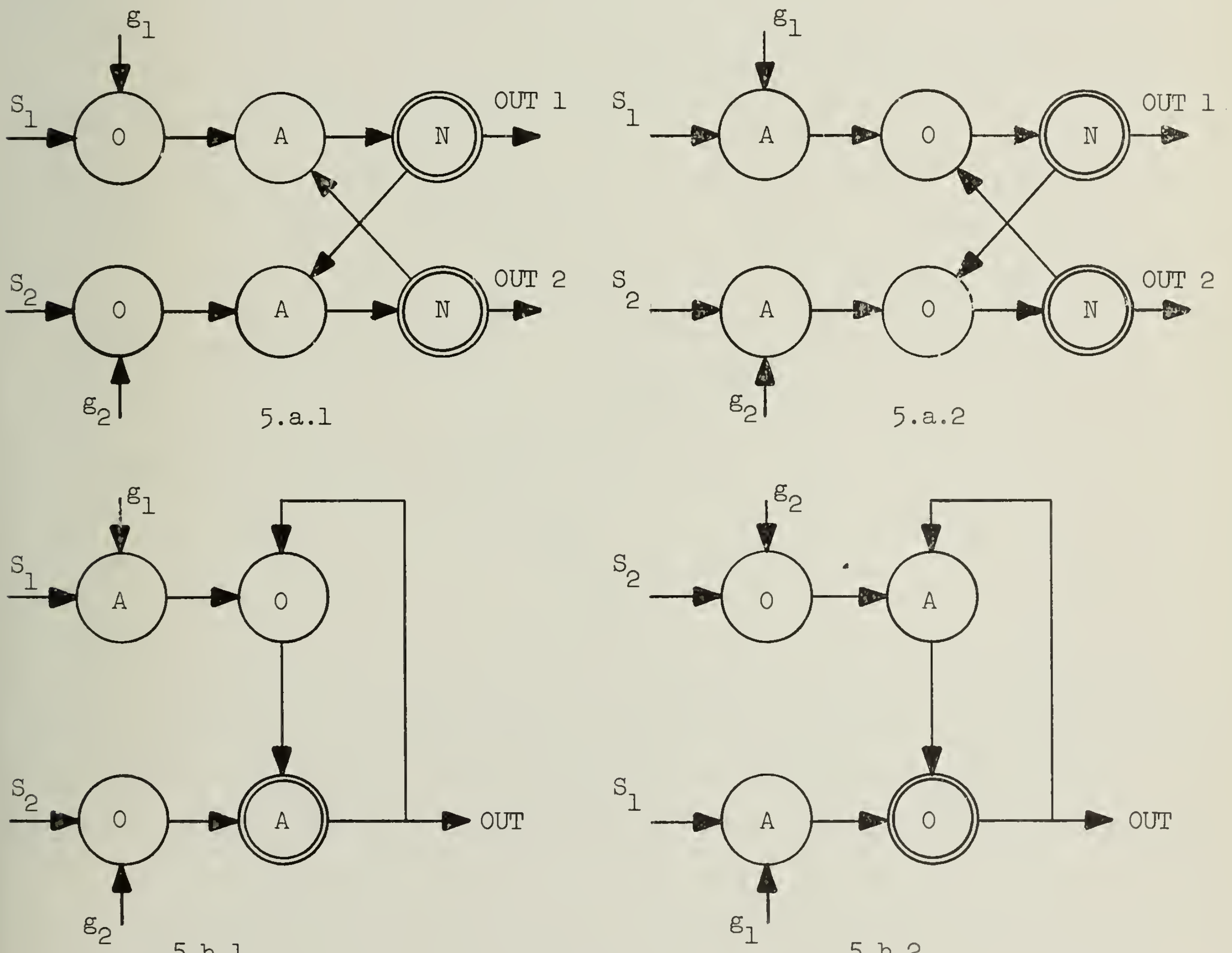
Table I gives details of operation of these flipflops for steady state inputs. For completeness, behavior under an input combination which is not legitimate is included as well. In fact, in the discussion that follows, the input combination when both inputs are active is an allowed state for the Eccles Jordan.

TABLE I

Figure	Flip-flop Type	Input Terminal	Quiescent Value	Behavior Under Various Input Conditions					
					Inputs		Outputs		State of Flipflop
4.a.1	Eccles Jordan	a	1		a	b	A	B	
		b	1	Legitimate Input Combinations	1	1	-	-	Remembers previous state
					0	1	1	0	1
					1	0	0	1	0
				Other	0	0	1	1	No memory, no state defined
4.a.2	Eccles Jordan	c	0		c	d	C	D	
		d	0	Legitimate Input Combinations	0	0	-	-	Remembers previous state
					1	0	0	1	0
					0	1	1	0	1
				Other	1	1	0	0	No memory, no state defined
4.b.	Schmidt	e	0		e	f	E		
		f	1	Legitimate Input Combinations	0	1	-		Remembers previous state
					0	0	0		0
					1	1	1		1
				Other	1	0	0		No memory, no state defined
4.c.	Schmidt	g	1		g	h	F		
		h	0	Legitimate Input Combinations	1	0	-		Remembers previous state
					1	1	1		1
					0	0	0		0
				Other	0	1	1		No memory, no state defined

Flipflops with Gates

It was stated earlier that a flipflop can be made to change its state by breaking the feedback loop at some convenient point and impressing the appropriate signal into it so that when the feedback loop is rejoined, the new state is latched onto. The circuits described in the previous section had the common feature that both the functions of initially breaking into the feedback loop and impressing the desired signal into the flipflop were performed by the same signal. The feedback loop was rejoined automatically, it will be noticed, in each case. It is usually desirable, however, to provide a "gate" to connect or disconnect the flipflop and the information source. This feature is incorporated into the flipflops of Figure 5.


g_1
S_1
O
A
N
OUT 1
S_2
O
A
N
OUT 2
g_2
g_1
S_1
A
O
N
OUT 1
S_2
A
O
N
OUT 2
g_2
g_1
S_1
A
O
S_2
O
A
OUT
g_2
g_2
S_2
O
A
S_1
A
O
OUT
g_1

5.a.1

5.a.2

5.b.1

5.b.2

Figure 5

Clearing and Gating

The flipflops in the previous section all have the common feature that though the information sources can be connected or disconnected to the flipflop at will by means of the gate, there are two signal inputs, one to be operative for each desired final state. It is in general desirable to have a single input whose value determines the state of the flipflop when the gate is open.

One way of accomplishing this is to have a "clear" input without a gate, which when activated takes the flipflop to the state 1. When the gate is activated, the flipflop either remains in the same state (1) or changes state (to 0) depending on the signal input value. There is the disadvantage in this system however that changing the state of a flipflop now requires two separate actions of clearing and gating, with correspondingly increased time of operation and circuit complexity.

For example, Figure 6 shows a flipflop derived from Figure 4.b., with provisions for clearing and gating.

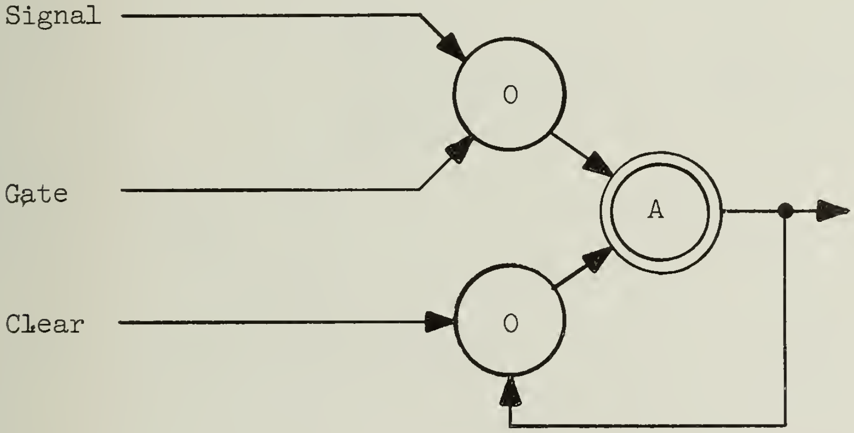


Figure 6

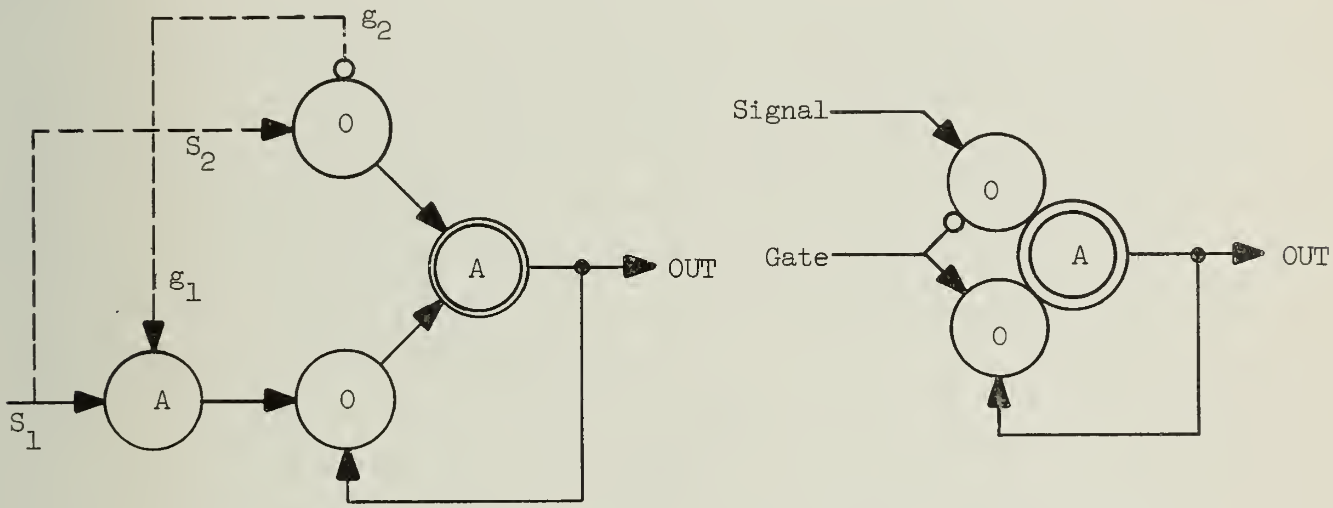
The quiescent values are 1 for the gate, 0 for the clear and signal. Changing state of the flipflop would consist of making the clear input 1 so that the flipflop is cleared to 1, and impressing a 0 on the gate input so that flopflop changes state to 0 if the signal input is 0, and remains in 1 otherwise.

The F-element

It will be noticed that the two flipflops in Figure 5.b. are substantially the same. Taking this information into account, and following the convention that a gate is quiescent when its value is zero, and that the state

of the flipflop is defined by the value of its output, these flipflops in Figure 5.b. can be standardized as in Figure 7.a. The round-headed arrow indicates an inverting input, and the broken lines that these inputs can be joined as indicated, optionally.

The commonly used F-element is of the form shown in Figure 7.b., and is derived from that of Figure 6 by following the conventions that the quiescent state of an input is 0, and by joining together the clear and gate terminals. The general operation of this F-element is somewhat similar to that of Figure 7.a. The requirements of the previous action regarding the sequential rather than simultaneous activation of the gate and clear input are no longer satisfied because these two inputs have been joined together. It is thus possible that race conditions might occur.

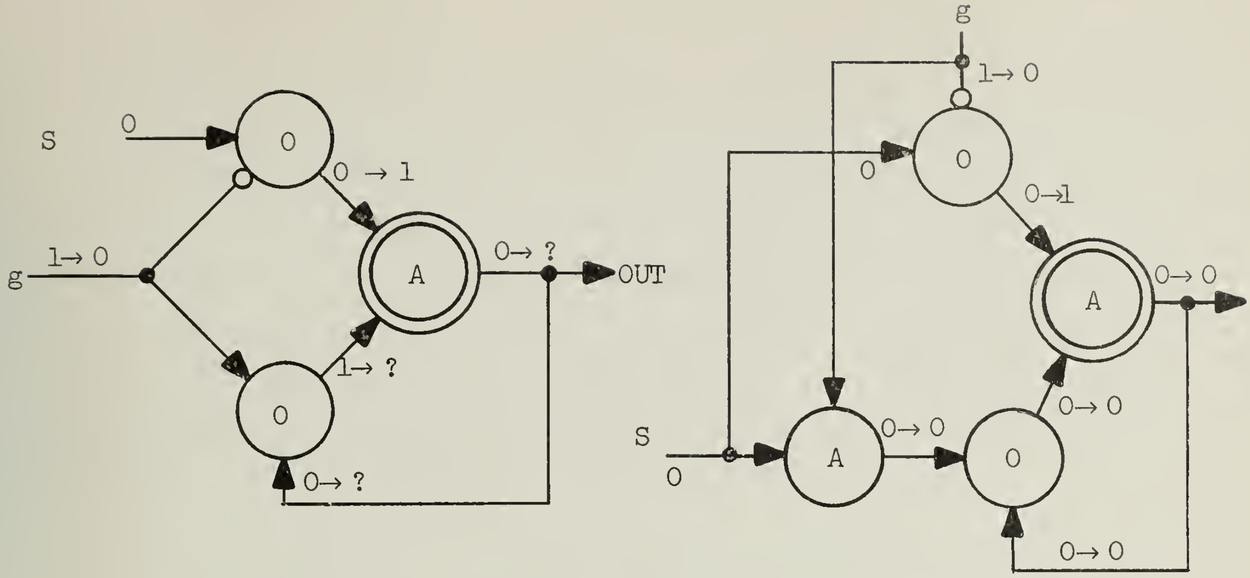


7.a. A Generalized F-element

7.b. The F-element

Figure 7

For instance, if the input is zero and the gate 1, the output is 0, but the flipflop has not yet attained a final state. For, when the gate changes from 1 → 0, (Figure 8) the two inputs to the restoring "AND" are changing in opposite directions, and the outcome could depend on the speeds of operation of the various elements in the circuit. Also, if the gate changes from 1 → 0 so slowly that the two inputs of the restoring "AND" remain in an "undeterimined state" for a time longer than the delay around the feedback loop of the flipflop, information could be lost. This defect doesn't exist in the more elaborate version of the F-element shown in Figure 8.b.


S
0
0
0 → 1
g
1→ 0
A
0→ ?
OUT
0
1→ ?
0→ ?
g
1→ 0
0
0
0→1
A
0→ 0
S
0
A
0→ 0
0
0→ 0
0→ 0

8.a. F-element 8.b. Generalized F-element

Figure 8 Transient Behavior of the F-element

This defect in the F-element can be safeguarded against by making sure that in the circuit of Figure 9, which is the F-element with the feedback loop opened up, the output is zero for all values of g (1, 0, or undetermined). This involves equality of speed of operation of the two nonrestoring "OR's", and also that the restoring "AND" gives an output 0, when g is in the "undetermined" region between 1 and 0. These conditions are satisfied by the logical circuits used in its construction.

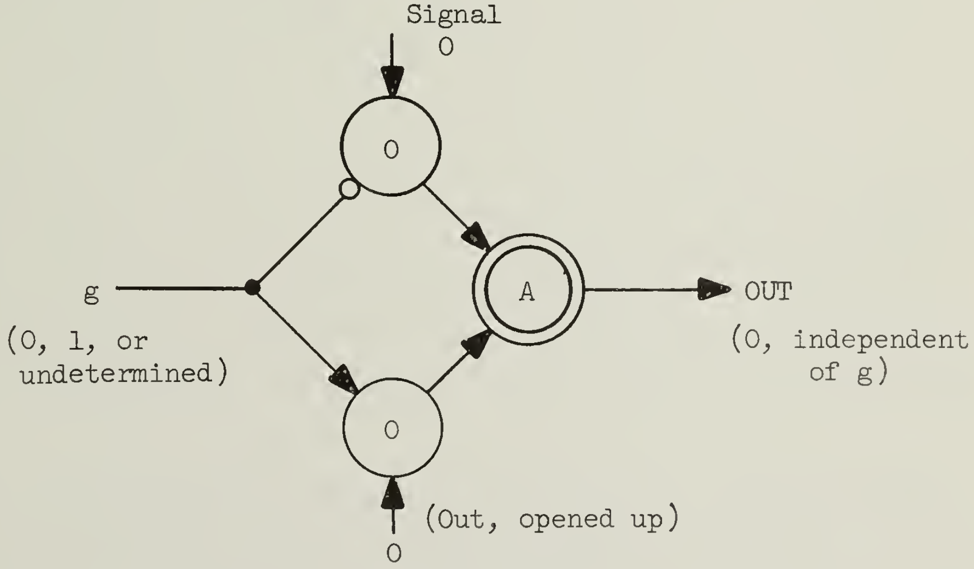

Signal
0
0
g
(0, 1, or undetermined)
A
OUT
(0, independent of g)
0
(Out, opened up)
0

Figure 9

The Eccles Jordan

The standard Eccles Jordan of the type generally used in ILLIAC II, is typically without gates and is either of the type shown in Figure 4.a.1 or 4.a.2. These have the property of unambiguous last moving point outputs.* For instance, in Figure 4.a.1., if input a changes from 1 to 0, output A changes from 0 to 1, and output B from 1 to 0, in that sequence. When B changes state in this case, the change of state in the flipflop is complete and B is thus the last moving point. A reply signal from B can, therefore, be used in a speed independent control logic to trigger the next operation.

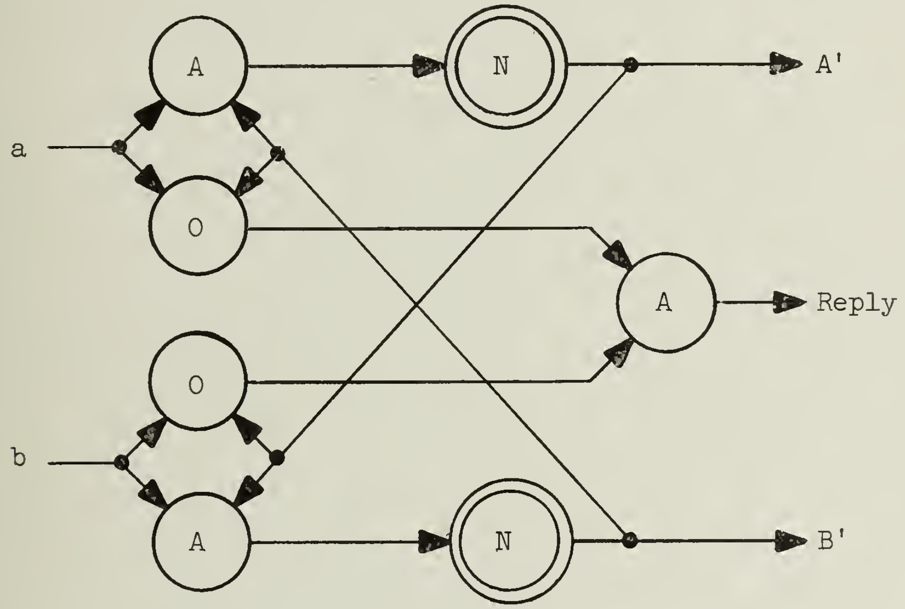


Figure 10 Eccles Jordan with Reply

This property is used in the Eccles Jordan with reply in Figure 10. Since the active input and the last moving output both attain the same state when the flipflop has attained a stable state, this causes the reply output to become a 0, signifying that the flipflop has changed state, and to become a 1 after the two inputs become 1. A similar circuit is possible for the OR-NOT flipflop.

Another common use for the Eccles Jordan is as a decision element when, say, a control sequence involves a choice between two possible courses of action, depending on the situation. For example, when access is requested

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* The Eccles Jordan used in ILLIAC II is topologically slightly different from these, and this strong statement is not entirely true in that case.

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of the core memory by two parts of the machine, the main Arithmetic Unit and the Magnetic Drum, say, the inputs are initially 0, and the outputs 1. The flipflop doesn't have memory in this state. When one of the inputs changes to 1 (requesting access) before the other, the opposite output changes to 0, and the flipflop remains locked in this state, signifying that the choice has been made in favor of the earlier contender. The inputs change back to 0 finally, bringing it back to the initial state.

In case both the inputs change simultaneously to a 1, the Eccles Jordan still attains a final state in a more or less random manner, in accordance with the requirement that as long as it is unambiguous, the actual final choice is unimportant.

There exists the likelihood, however, under these circumstances, i.e. when both inputs are simultaneously turned to 1, that the two outputs might oscillate in phase, with a frequency determined by the delay in the feedback loop. This is true because in this case the conditions are similar to those in a "logical oscillator" consisting of a restoring "not" with the output and input tied together. Since this behavior is inherent to its structure, the best that can be hoped is to minimize this tendency, and its possible effect on the external circuitry. If, for instance, the duration of this oscillation is minimized, so that the final decision is reached without two much delay and also during this period, the external circuitry is prevented from false interpretation of the state of the flipflop, there is no hazard. This is accomplished by

(1) Reducing the delay in the feedback loop so as to decrease the period and hence amplitude of oscillation as the frequency response of the circuitry is limited. If the rise time of the input signal is small compared to the period of oscillation, simultaneity of inputs and consequently the likelihood of oscillation decreases.

(2) Separating the feedback outputs (supplying the AND circuits) and the actual outputs that communicate with the external world, and arranging by means of shifted thresholds that expected internal oscillation is not communicated to the circuits fed by the element.

Flow Gating

It is very convenient to have a bank of registers (Index Registers, say) that have the property that information can be transferred from any one of these registers to any other. Standard methods of gating require individual gating paths between each pair of registers, making this arrangement impractical for a reasonable number of registers. The following pages describe a memory element meeting the above requirement, but using only a single common information bus per bit, rather than have $2x^{n}C_{2}$ information paths. This system involves the use of "selectors" or "isolators" both at the input and output of each memory element. The output of the selected memory element is fed to the common signal bus, and from there on to the second memory element which is to be set. Though such an arrangement is conceivably possible for other types of flipflops as well, the system to be discussed presently is considerably more economical than others known.

The Flowflop

Going back to the section entitled General Discussion, it is recalled that a flipflop can be made to change state by changing the state of any of the nodes in the feedback loop by brute force methods. This implies that the circuit driving any of these nodes from one state to the other must have an output impedance which is lower than the input impedance of the memory element at that point. Furthermore, since the flipflop is required to "remember" its state after being so driven,the "driver" should get disconnected from the node until such time when another change of state is desired. Conventional methods of gating accomplish precisely this. The state of each node of the flipflop being in general a function of the state of the flipflop, these conditions are satisfied more easily if two nodes are used for this purpose, one for each desired final state. If, on the other hand, this gating is desired to be accomplished at a single node, two separate circuits are required to impress a change into one state or the other. Figure 11 which is a combination of circuit and logic symbols, is one such.

S is the signal input which connects itself to the input point of the flipflop when g is positive (or $\bar{g}$ negative) and not otherwise. Since the object of this gating is to change the potential of one base with respect to the other, a simpler method would be to vary the potential of the base presently

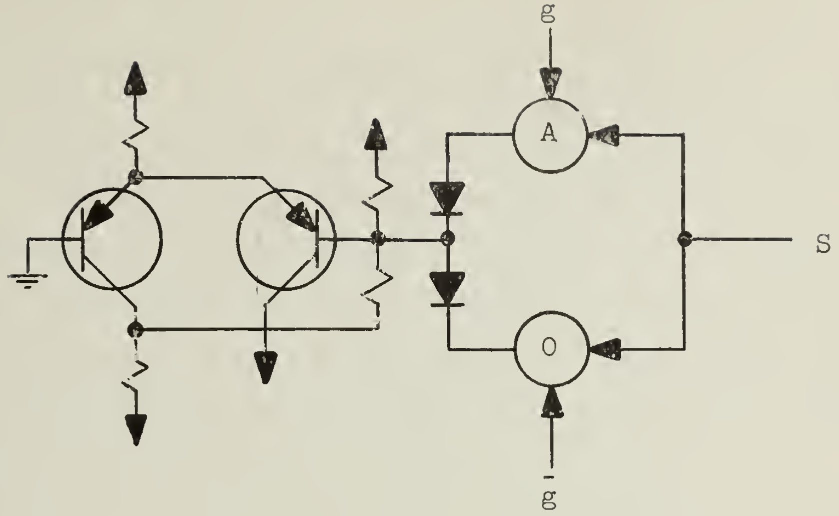


Figure 11

connected to ground. Since the feedback path to the other transistor goes only through the emitter circuit, there is the advantage of speed. In this configuration, where the input is impressed on the left base, the setup is a Schmidt Trigger Unit. Changing the state of the circuit is accomplished by the circuit of Figure 12.

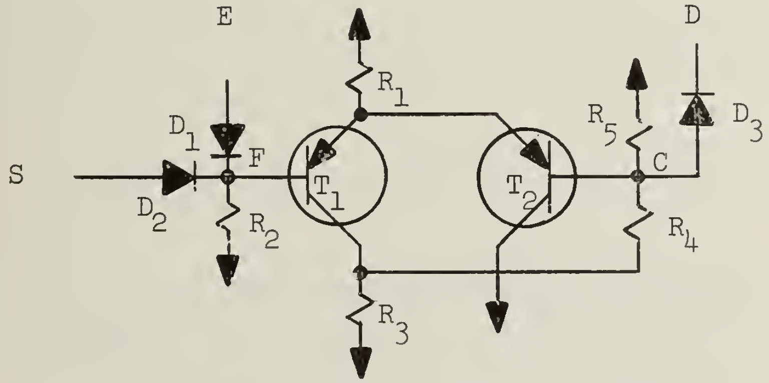

E
D
S
D_1
D_2
F
R_1
R_2
R_3
T_1
T_2
R_5
C
R_4
D_3

Figure 12

Gating is accomplished when E and D are both low. Their values are such that if the input is 1, S and F are more positive than C, so that the transistor T_2 conducts, and when the input is zero, S and F are more negative than C, and T_1 conducts. In the normal "storage" state, diodes D_2 and D_3 are out of conduction, and the flipflop is free to retain whatever state it originally was in. The question arises, therefore, whether or not the impressed state is remembered by the flipflop during the transition from "gating" to "storage" states. This depends in turn on whether or not the emitter-base diode of the conducting transistor becomes reverse biased during transition, and if it does, whether this condition remains long enough for the base charge to disappear, making the transistor drop out of conduction.

The notation to be adopted in the following pages is as follows:

(1) Unless otherwise specified, names of the nodes with subscripts indicate the respective node voltages.

(2) The three states of each node, gating, transient and storage are denoted by the first subscript, as g, t, or s. In case of the transient state, node voltages which vary with time are expressed as functions of time $E_t(t)$, etc.

(3) The second subscript (1 or 0) indicates the state of the flipflop.

(4) Either subscript is dropped if the node voltage remains constant for all possible values of the subscript.

(5) Overline and underline indicate the maximum and minimum tolerance range for the voltage at the node under worst case conditions. Without either, the voltage indicates the typical value.

(6) The forward voltage drop across a conducting diode D_i is represented as V_{Di}.

Using these conventions, and from the properties of the element that are already enumerated:

$$D_{s0} = D_{s1} = D_s \tag{1}$$

$$E_{s0} = E_{s1} = E_s \tag{2}$$

$$D_{t0}(t) = D_{t1}(t) = D_t(t) \tag{3}$$

$$E_{t0}(t) = E_{t1}(t) = E_t(t) \tag{4}$$

Equations (1) through (4) hold because the driver voltage is supposedly independent of the flipflop behavior, since the input signal value

$$S_{g0} = S_{t0}(t) = S_{s0} = S_0 \tag{5}$$

$$S_{g1} = S_{t1}(t) = S_{s1} = S_1 \tag{6}$$

does not depend on the state of the flipflop.

Let us consider, to start with, the flowflop in the gating state, the input signal being negative for a zero input. The voltages of the various nodes are enumerated in Figure 13. D is more positive than E, though both are much more negative than their normal values during "store" state. The diode D_1 or D_2 conducts depending on which one of the two voltages E_g or S_0 is less negative. (In the case shown, $E_g < S_0$). Diode D_3 is in conduction, and transistor T_1 is in condution, its base being more negative. In the absence of diode D_3, C would have been at a level C'_g indicated by the dotted line, due to differential amplifier action. Flipflop action would still have been present. The existence of this diode holds the voltage on C to the immediate more positive neighborhood of D, determined by its forward drop. The circuit is no longer a flipflop, since the collector base feedback from T_1 to T_2 is destroyed by the conduction of D_3.

In the transient state, when E and D move towards their "store" state values, assuming a linear increase, F remains in the neighborhood of S_0 unti $E_t(t)$ catches up with S_0, and then follows E_1 as D_1 starts conduction cutting off D_2. F reaches its steady state value (F_{s0}) as soon as E does, (E_s) D_1 still conducting. Again, had D_3 been absent, C, as indicated by C' would have steadily fallen as F rose, reaching its steady state value (C_{s0}) for store 0 as soon as F did. Since diode D_3 is in conduction, C follows $D_t(t)$ on the path indicated, until it intersects the dotted line C', at which point D_3 drops out of conduction. Flipflop action is restored and C, from this point, follows the path it would have, in the absence of D_3, finally attaining the level C_{s0}. With neither of the diodes D_2 and D_3 conducting, whatever the state of S, (S_1 or S_0), the flipflop retains this state.

Considering the case now where a 1 is to be gated in, since S_1 is more positive than E_g, diode D_1 conducts, and F_{g1} is slightly more negative

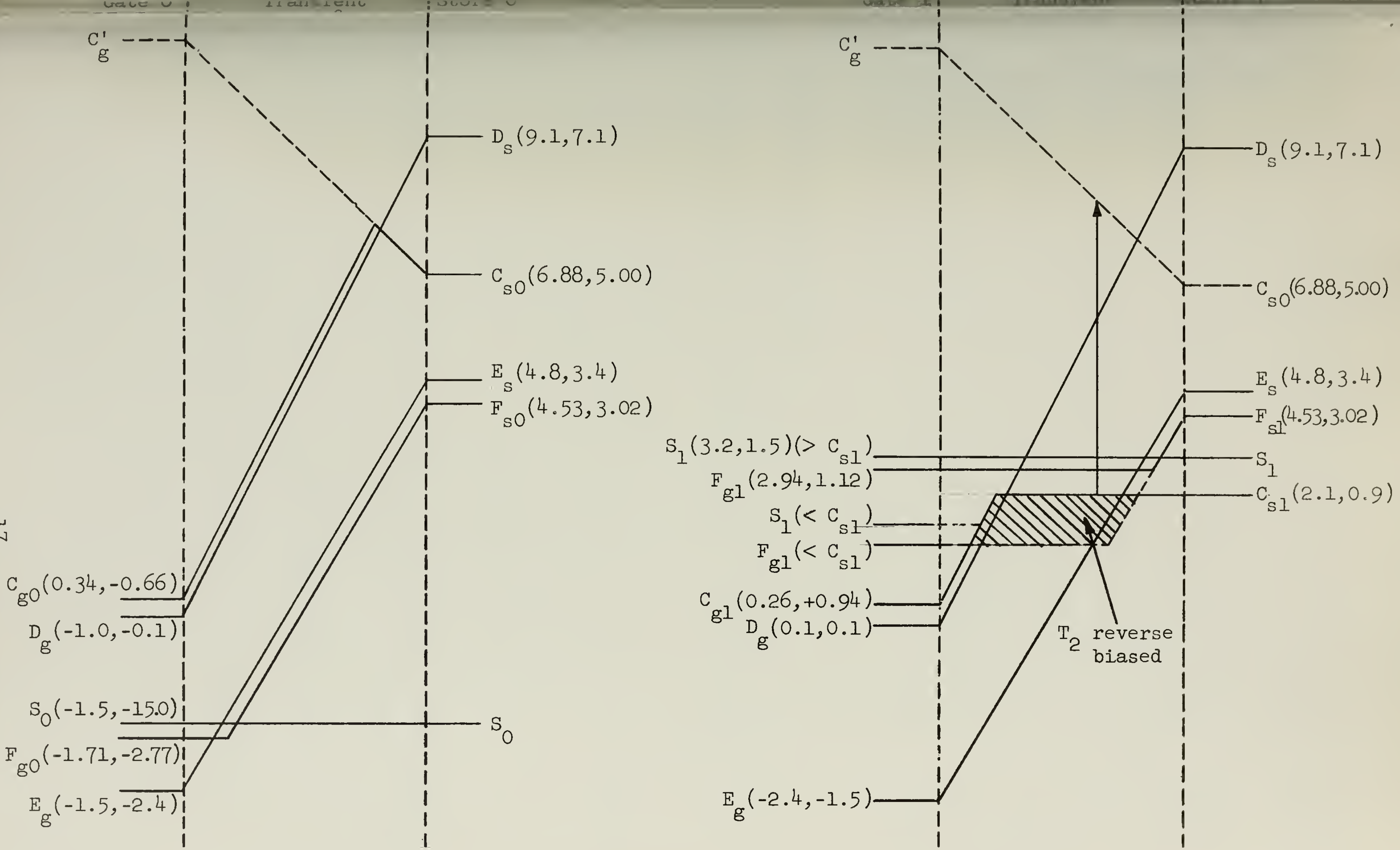

C'_g
$D_s(9.1,7.1)$
$C_{s0}(6.88,5.00)$
$E_s(4.8,3.4)$
$F_{s0}(4.53,3.02)$
S_0
$C_{g0}(0.34,-0.66)$
$D_g(-1.0,-0.1)$
$S_0(-1.5,-15.0)$
$F_{g0}(-1.71,-2.77)$
$E_g(-1.5,-2.4)$
C'_g
$D_s(9.1,7.1)$
$C_{s0}(6.88,5.00)$
$E_s(4.8,3.4)$
$F_{s1}(4.53,3.02)$
S_1
$C_{s1}(2.1,0.9)$
$S_1(3.2,1.5)(> C_{s1})$
$F_{g1}(2.94,1.12)$
$S_1(< C_{s1})$
$F_{g1}(< C_{s1})$
$C_{g1}(0.26,+0.94)$
$D_g(0.1,0.1)$
$E_g(-2.4,-1.5)$
T_2 reverse biased

Figure 13 Transient Behavior of the Flowflop

Notes: 1. The voltage levels are approximately to scale.

2. The numbers in parentheses indicate the spread in the node voltages due to component tolerance, etc., on a worst case basis. (Drawing B-990)

than S_1. D_3 will be conducting if C'_g, the value of C in the absence of D_3 while gating a 1, is more positive than D_g. In either case F_{g1} is more positive than C_{g1} leaving T_1 cut off.

As E and D go from the gating to store level, F follows $E_t(t)$ as soon as $E_t(t)$ crosses S_1. Since T_1 is off, variation of $F_t(t)$ is without effect on C_{t1}. C_{t1} follows D until D crosses C_{s1} and then, as D_3 turns off, remains at that level. F finally remains at F_{s1}, diode D_1 still conducting.

If, however, F_{g1} is not more positive than C_{s1}, there is some danger of C_{t1} crossing F_{g1} before E_t catches up with F_{g1}. Since the conducting transistor, T_2, is reverse biased in this region, there is the danger of this transistor dropping out of conduction, reversing the state of the flipflop, if this condition persists long enough, i.e., longer than the switching time of the transistor.

Some Design Considerations

From the above discussion, it follows that the following conditions should be satisfied for successful operation of the flowflop.

(1) State 0

During gating, $\overline{F_{g0}} < \underline{C_{g0}}$ for transistor T_1 to conduct.

This implies that $$\overline{S_0} - \underline{V_{D2}} < \underline{D_g} + \underline{V_{D3}} \qquad (7)$$

and $$\overline{E}_g - \underline{V_{D1}} < \underline{D_g} + \underline{V_{D3}} \qquad (8)$$

During the transition to "store" state, $\overline{F_{t0}(t)} < \underline{C_{t0}(t)}$ to prevent T_1 from dropping out of conduction. Thus,

$$\overline{E_t(t)} - \underline{V_{D1}} < \underline{D_t(t)} + \underline{V_{D3}} \qquad (9)$$

During storage, for the state to be remembered,

$$\overline{F}_{s0} < \underline{C_{s0}} ,$$

i.e., $$\overline{E}_s - \underline{V_{D1}} < \underline{C_{s0}} , \qquad (10)$$

and for flipflop action to be retained by preserving the collector base feedback, D_3 should be out of conduction, so that

$$\overline{C_{s0}} < \underline{D_s} \qquad (11)$$

It is essential for the flipflop not to be disturbed by the variations in input, so that

$$\underline{F_{s0}} > \overline{S_1} \text{ or } \overline{S_0}$$

i.e.,

$$\underline{E_s} - \overline{V_{D1}} > \overline{S_1} \qquad (12)$$

(2) State 1

During gating, $\underline{F_{g1}} > \overline{C_{g1}}$ for transistor T_2 to conduct, i.e.,

$$\underline{S_1} - \overline{V_{D2}} > \overline{D_g} + \overline{V_{D3}} \qquad (13)$$

During transients, preferably, the conducting transistor T_2 should not be reverse biased, i.e.,

$$\underline{F_{t1}(t)} > \overline{C_{t1}(t)}$$

$$\underline{F_{g1}} > \overline{C_{s1}} \qquad (14)$$

During storage, for retention of the state,

$$\underline{F_{s1}} > \overline{C_{s1}}$$

i.e.,

$$\underline{E_s} - \overline{V_{D2}} > \overline{C_{s1}} \qquad (15)$$

Equation (12) insures that D_2 is cut off even in this state. For D_3 to be cut off, isolating the flowflop from D,

$$\overline{C_{s1}} < \underline{D_s} \qquad (16)$$

(3) To assure efficiency of gating, the mean voltage in E_C should be at the center of the gate-in band.

$$\frac{\bar{C}_g + \underline{C}_g}{2} = \frac{1}{2} \left(\frac{\bar{F}_{g1} + \underline{F}_{g1}}{2} + \frac{\bar{F}_{g0} + \underline{F}_{go}}{2} \right) \tag{17}$$

For further details regarding the design of a flowflop, reference may be made to Report No. 106.

Readout

A requirement stated earlier is that the stored signal is to be made available on demand so that a common output bus suffices for each bit for transfer of information between any two registers in a bank of registers. To ensure proper gating of information from one flowflop to another, the minimum guaranteed outputs in both states should be such as to satisfy the conditions imposed on the input signal as enumerated in the previous section. The final design of the flowflop is shown in Figure 14 (B-990). Read gating is effected by lowering R.

To summarize the operation of the "flowflop",

(1) It is a difference amplifier during gating.

(2) It is a Schmidt Trigger during storing.

(3) The linearity properties of the difference amplifier enable the transition from gating to storing. The storage properties of transistors (i.e., finite cut-off time) aid this transition, lending it extra stability.

NOTES

1. In flow flop proper, "Gate" refers to "write".
   At output, "Gate" refers to "read out".
2. All voltages and currents are D. C. static values.
3. The first row of the listing is node voltages.
   The second and third rows are branch currents.
   These are read as node in the first row, (to, from)
   node in the second or third row, or as indicated directly.
4. This resistor is equal to 4 resistors of 8k 1/2w, ± 1%
   in parallel. (see output bus drawing.)

Power Supplies

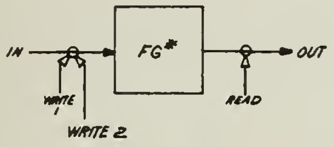
+25v	52	ma.	max.	reqd.
+6.8v	-	-	-	-
-5v	28	"	"	"
-50	37	"	"	"
-13.5v	6	"	"	"

# Stabistor supplies not included.

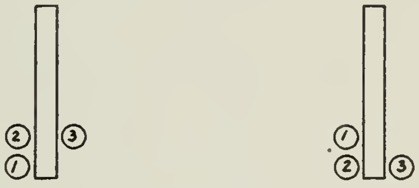
When Not Specified

(Design tolerance ± 3%)
Resistors ± 1%, 1/2 w.
Transistors (GF45011) see file no. 316
or (N-100) see report
Diodes (S570) see file no. 317
For bump voltage supplies see dwg. B947

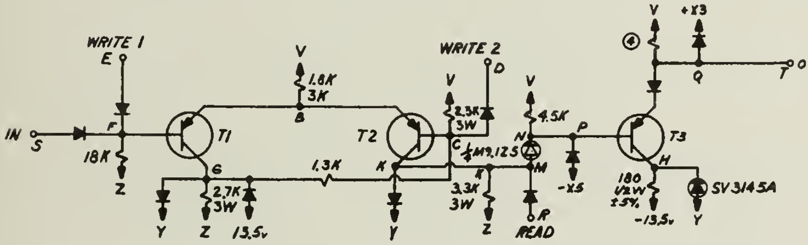
V = +25v.
Y = -5v.
W = +6.8v.
Z = -50v.



SYMBOL



LAYOUT



③

GF450II

V		B		C		S		E		F		G		-13.5v		Y-(-5)		K		N		Q		D			
25.75 24.25		-2.54 -1.11	0.844 -.713	0.34 -0.66	0.259 -0.944	-15.0 -1.5	3.2 1.5	-2.4 -1.5	-2.4 -1.5	2.77 -1.72	2.98 1.12	-6.59 -4.46	-14.4 -13.4	-13.9 -13.1		-5.1 -4.9		-14 -10	-4.93 -4.4	-3.93 -3.3	5.5 3.5	-3.0 -2.3	3.05 2.6	-1.0 -0.1	0.1 0.1		
		5.09 3.25	2.68 -0.671	6.88 5.00	2.11 -0.901	-15.0 -1.5	3.2 1.5	4.8 3.4	4.8 3.4	4.53 3.02	4.53 3.02	-5.37 -4.43	-14.4 -13.4					-4.82 -4.37	-4.72 -4.2	5.53 3.6	5.65 3.7	3.05 2.6	3.05 2.6	9.1 7.1	9.1 7.1		
to B		T-1(Coll)		to G		to F		to F		to Z		to Z		to C		from G		from Z		to M		from V		from C			
16.2 13.7	15.2 12.7	16.2 12.7	0 0	4.76 2.86	11.4 9.42	1.43 0	3.11 2.67	1.43 1.34	0 0	2.85 2.46	3.11 2.67	17.84 15.73	14.54 12.33	0 0	5.09 0.879	4.5 0	0 0	12.5 10.2	14.6 13	12.5 10	4.7 4.4	14.8 12.9	11.6 10	8.95 5.34	3.44 0		
12.9 10.6	15.1 11.7	12.9 9.62	0 0	8.75 7.73	12.1 10.1	0 0	0 0	3.21 1.88	3.20 2.78	3.21 2.78	3.20 2.78	17.84 15.73	14.54 13.56	0 0	4.39 0.284	5.93 0	0 0	15 13	15 13	5.0 4.0	5.0 4.0	14.8 12.9	11.6 10	0 0	0 0		
to C		T-2(Coll)		T_3 Base		R T O M		Q to X_3		X_5 to P		T-3 Emitter		from H		from K		from M		from V		from or to T		T_3 (Coll)		Y to H	
11.8 10.1	11.9 10.1	0 0	15.2 11.7	1.2 0	0 0	0 0	0 0	0 0	11.9 10.2	5.5 2.2	0 0	16.8 12.9	0 0	35 25	36.2 22.6	0 0	6.75 0.7	12.5 10.2	4.7 4.4	6.8 5.9	5.0 4.7	2.2 0.4	2 0.4	19.2 12.1	0 0	22.9 5.7	36.2 22.6
8.79 7.74	12.1 9.79	0 0	15.1 10.8	0 0	0 0	19.2 16.5	20.5 17.3	11.9 10.2	11.9 10.2	0 0	0 0	0 0	0 0	35 25	36.2 22.6	10.7 5.38	28 18	23.7 20.9	25.6 21.7	5.0 4.0	5.0 4.0	2.2 0.4	2 0.4	19.2 12.1	0 0	22.9 5.7	36.2 22.6

①

Gate "0"	Gate "I"
Store "0"	Store "I"

N-100

V		B		C		S		E		F.		G		-13.5v		Y(-5v)		K		N		Q		D			
25.75 24.25		-2.65 -1.26	0.690 -0.723	0.345 -0.658	0.259 -0.944	-15.0 -1.5	3.2 1.5	-2.4 -1.5	-2.4 -1.5	-2.77 -1.71	2.93 1.13	-6.51 -4.46	-14.41 -13.36	-13.9 -13.1		-5.1 -4.9		-14 -10	-4.93 -4.4	-3.93 -3.3	5.5 3.5	-3.0 -2.3	3.05 2.6	-1.0 -0.1	-1.0 -0.1		
		4.93 3.24	2.53 -0.681	6.88 5.1	2.12 -0.901	-15.0 -1.5	3.2 1.5	4.8 3.4	4.8 3.4	4.53 3.02	4.5 3.02	-5.26 -4.43	-14.41 -13.34					-4.82 -4.37	-4.72 -4.25	5.53 3.6	5.65 3.7	3.05 2.6	3.05 2.6	9.1 7.1	9.1 7.1		
to B		T-1(Coll)		to G		to F		to F		to Z		to Z		to G		From G		From Z		To M		From V		From C			
16.21 13.77	15.16 12.72	17.95 15.65	0 0	4.71 2.86	11.49 9.43	1.42 0	3.12 2.68	1.43 1.34	0 0	2.85 2.46	3.12 2.68	17.95 15.69	14.55 12.31	0 0	5.09 0.879	4.6 0	0 0	12.5 10.2	14.6 13.0	12.5 10.0	4.7 4.4	14.8 12.9	11.6 10.0	8.99 5.39	3.44 0		
12.89 10.43	15.14 11.78	17.96 15.68	0 0	8.79 7.74	12.09 10.15	0 0	0 0	3.21 1.88	3.21 2.71	3.21 2.78	3.21 2.71	17.96 15.68	14.56 13.56	0 0	4.39 0.28	5.92 0	0 0	15.0 13.0	15.0 13.0	5.0 4.0	5.0 4.0	14.8 12.9	11.6 10.0	0 0	0 0		
to C		T-2(Coll)		T-3 Base		R to M		Q to X_3		X_5 to P		T-3 Emitter		From H		From K		From M		From V		From To T		-3 (Coll)		Y to H	
11.83 10.1	11.89 10.14	0 0	15.16 11.83	1.2 0	0 0	0 0	0 0	0 0	11.9 10.2	5.5 2.2	0 0	16.8 12.9	0 0	35 25	36.2 22.6	0 0	6.75 0.7	12.5 10.2	4.7 4.4	6.8 5.9	5.0 4.7	2.2 0.4	2.0 0.4	19.2 12.1	0 0	22.9 5.7	36.2 22.6
8.79 7.74	11.46 9.79	0 0	15.14 10.83	0 0	0 0	19.2 16.5	20.5 17.3	11.9 10.2	11.9 10.2	0 0	0 0	0 0	0 0	35 25	36.2 22.6	10.7 5.38	28 18	23.7 20.9	25.6 21.7	5.0 4.0	5.0 4.0	2.2 0.4	2.0 0.4	19.2 12.1	0 0	22.9 5.7	36.2 22.6

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FLOW FLOP

FLOW GATING CIRCUIT

B990

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